CTLT3410-M621 (NPN)
CTLT7410-M621 (PNP)

SURFACE MOUNT
COMPLEMENTARY SILICON
LOW $V_{CE\ (SAT)}$ TRANSISTORS

Top View Bottom View

TLM621

Central™
Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLT3410-M621 and CTLT7410-M621 are Low $V_{CE\ (SAT)}$ transistors in a very small leadless 1x2mm surface mount package, designed for applications where small size, operational efficiency, and low energy consumption are prime requirements. Due to the leadless package design, these devices are capable of dissipating up to 3 times the power of similar devices in comparable sized surface mount packages.

CTLT3410-M621 MARKING CODE: CB
CTLT7410-M621 MARKING CODE: CD

APPLICATIONS:

- DC/DC Converters
- Switching Circuits
- LCD Backlighting
- Battery Powered Portable Equipment

FEATURES:

- High Operational Efficiency
- High Power to Footprint Ratio
- $V_{CE(SAT)}$ @ 1.0A = 250mV (TYP)
- High Collector Current
- Small TLM621 1x2mm Package

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Collector-Base Voltage	V_{CBO}	40	V
Collector-Emitter Voltage	V_{CEO}	25	V
Emitter-Base Voltage	V_{EBO}	6.0	V
Collector Current	I_C	1.0	A
Collector Current (Peak)	I_{CM}	1.5	A
Power Dissipation (See Note 1)	P_D	0.9	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (See Note 1)	Θ_{JA}	139	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**		**MAX**	**UNITS**
			PNP	**NPN**		
I_{CBO}	V_{CB}=40V				100	nA
I_{EBO}	V_{EB}=6.0V				100	nA
BV_{CBO}	I_C=100µA	40				V
BV_{CEO}	I_C=10mA	25				V
BV_{EBO}	I_E=100µA	6.0				V
$V_{CE(SAT)}$	I_C=50mA, I_B=5.0mA		.02	.025	.05	V
$V_{CE(SAT)}$	I_C=100mA, I_B=10mA		.035	.04	.075	V
$V_{CE(SAT)}$	I_C=200mA, I_B=20mA		.075	.08	0.15	V
$V_{CE(SAT)}$	I_C=500mA, I_B=50mA		0.13	0.15	0.25	V
$V_{CE(SAT)}$	I_C=800mA, I_B=80mA		0.2	0.22	0.4	V
$V_{CE(SAT)}$	I_C=1.0A, I_B=100mA		0.25	0.275	0.45	V
$V_{BE(SAT)}$	I_C=800mA, I_B=80mA				1.1	V
$V_{BE(ON)}$	V_{CE}=1.0V, I_C=10mA				0.9	V
h_{FE}	V_{CE}=1.0V, I_C=10mA	100				
h_{FE}	V_{CE}=1.0V, I_C=100mA	100			300	
h_{FE}	V_{CE}=1.0V, I_C=500mA	100				
h_{FE}	V_{CE}=1.0V, I_C=1.0A	50				
f_T	V_{CE}=10V, I_C=50mA, f=100MHz	100				MHz
C_{ob}	V_{CB}=10V, I_E=0, f=1.0MHz **(NPN)**				10	pF
C_{ob}	V_{CB}=10V, I_E=0, f=1.0MHz **(PNP)**				15	pF

Note 1: FR-4 Epoxy PCB with copper mounting pad area of 33mm^2

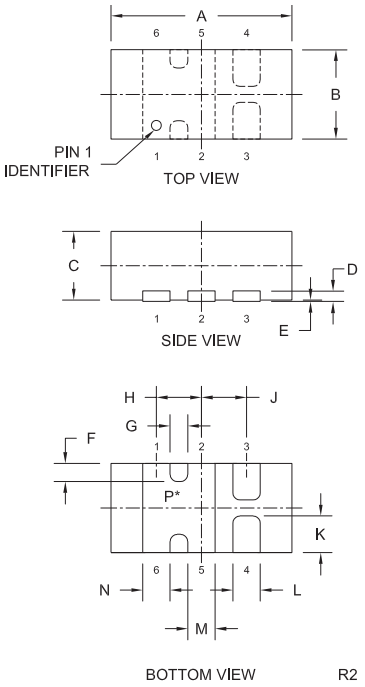
R0 (14-January 2008)

Central™
Semiconductor Corp.

CTLT3410-M621 (NPN)
CTLT7410-M621 (PNP)

SURFACE MOUNT
COMPLEMENTARY SILICON
LOW $V_{CE\ (SAT)}$ TRANSISTORS

TLM621 CASE - MECHANICAL OUTLINE

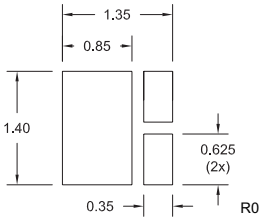


DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.073	0.085	1.850	2.150
B	0.033	0.045	0.850	1.150
C	0.028	0.031	0.700	0.800
D	0.006		0.150	
E	0.000	0.002	0.000	0.050
F	0.008		0.200	
G	0.010		0.250	
H	0.020		0.500	
J	0.020		0.500	
K	0.012	0.020	0.300	0.500
L	0.007	0.012	0.180	0.300
M	0.007	0.012	0.180	0.300
N	0.007	0.012	0.180	0.300

TLM621 (REV: R2)

SUGGESTED MOUNTING PADS

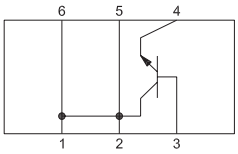
(Dimensions in mm)



* Exposed pad P connects pins 1, 2, 5, and 6

PIN CONFIGURATION

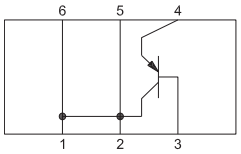
CTLT3410-M621



LEAD CODE:
1) Collector
2) Collector
3) Base
4) Emitter
5) Collector
6) Collector

MARKING CODE: CB

CTLT7410-M621



LEAD CODE:
1) Collector
2) Collector
3) Base
4) Emitter
5) Collector
6) Collector

MARKING CODE: CD

R0 (14-January 2008)